



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,362	07/08/2003	Lucy G. Hosking	9775-0157-999	2325

24341 7590 03/29/2005

MORGAN, LEWIS & BOCKIUS, LLP.  
2 PALO ALTO SQUARE  
3000 EL CAMINO REAL  
PALO ALTO, CA 94306

EXAMINER

LEUNG, CHRISTINA Y

ART UNIT PAPER NUMBER

2633

DATE MAILED: 03/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 10/616,362	Applicant(s) HOSKING ET AL.	
	Examiner Christina Y. Leung	Art Unit 2633	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 08 July 2003.
- 2a) ☐ This action is FINAL.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-11 and 13-22 is/are rejected.
- 7) ☒ Claim(s) 10 and 12 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>10-22-04; 1-28-05</u> | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Objections*

1. Claim 10 is objected to because of the following informalities:

Line 5 of claim 10 recites “a direct current (DC) bias signal....” Based on Applicants’ specification, Examiner respectfully suggests that Applicants amend the phrase to “a direct current (DC) bias *monitor* signal” in order to distinguish the signal from the “DC bias *control* signal” recited in other claims. Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 9 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 9 recites the limitation “said AC control signal” in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim, since claim 7 on which it depends does not previously recite an AC control signal. Examiner respectfully suggests that claim 9 may depend on claim 8 instead.

### *Claim Rejections - 35 USC § 102*

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 20 is rejected under 35 U.S.C. 102(b) as being anticipated by Kollanyi et al. (US 4,809,286 A).

Regarding claim 20, Kollanyi et al. disclose an optoelectronic transceiver (Figures 1 and 2) comprising:

- an optoelectronic transmitter (laser 160);
- an optoelectronic receiver (optical detector 110);
- a laser driver 170 electrically coupled to the optoelectronic transmitter;
- a post amplifier 120 electrically coupled to the optoelectronic receiver;
- a first controller integrated circuit (laser DC bias control 150) electrically coupled to the laser driver, where the first controller IC is configured to supply a direct current (DC) bias current control signal to the laser driver causing the laser driver to supply DC bias current to the optoelectronic transmitter (column 3, lines 45-48);
- a second controller IC (data driver 180) electrically coupled to the laser driver to supply an alternating current (AC) current control signal to the laser driver causing the laser driver to supply AC current to the optoelectronic transmitter (column 4, lines 17-24).

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1, 2, 4-6, 8, 9, 13-15, and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. (US 5,801,866 A) in view of King et al. (US 5,812,572 A).

Regarding claim 1, Chan et al. discloses an optoelectronic transceiver (Figure 4), comprising:

a first controller integrated circuit (transmit controller 116) and a second controller IC (receiver controller 128), each comprising logic.:

Chan et al. further disclose that each controller integrated circuit is connected to a corresponding memory element (memory 122 and memory 144), and further disclose that the memories are configured to store digital diagnostic data, where at least some of the digital diagnostic data is common to both the first controller IC and the second controller IC (column 5, lines 20-45). Chan et al. disclose that the first and second controllers may share information; Examiner notes that the claim does not specifically disclose specific details regarding the “diagnostic data.”

Chan et al. further disclose, for each controller IC, an interface electrically coupled to the memory and configured for communicating the diagnostic data to a host external to the optoelectronic transceiver (the multiple RS232 interfaces shown in Figure 4, for example); and at least one input port electrically coupled to the memory and configured to receive the diagnostic data from other components within the optoelectronic transceiver (i.e., the input ports coupled to the photodiode 112 or laser 90, for example)..

Chan et al. do not specifically disclose that each integrated circuit itself includes integrated memory, but it is well known in the art that a controller, particularly a controller comprising a microprocessor such as disclosed by Chan et al., may include memory as part of its integrated circuit. King et al. particularly teach an optoelectronic device related to the one disclosed by Chan et al. (Figure 1) including a controller 50 with logic and memory (Figure 1).

Regarding claim 6 in particular, King et al. further teach storing data in different memory mapped locations in memory within a controller (column 13, lines 58-67; column 14, lines 1-9).

Regarding claims 1 and 6, it would have been obvious to a person of ordinary skill in the art to use controllers with integrated memory as suggested by King et al. in the system disclosed by Chan et al. in order to provide a more compact system and allow the logic in the controllers to access internal memory quickly (instead of over external connections).

Regarding claim 2, Chan et al. disclose that the interface is a serial interface (i.e., RS232 serial interfaces).

Regarding claims 4 and 5, Chan et al. disclose other components including an transmitter/laser subassembly 90, a laser driver IC 94, and a receiver subassembly 112, for example.

Regarding claim 8, Chan et al. disclose a system as discussed above with regard to claim 1, and they further disclose that one of the controller ICs is electrically coupled to a thermoelectric cooler driver IC (temperature controller 54 in Figure 7, for example) to supply a TEC control signal (column 6, lines 63-66).

Further regarding claim 8, Chan et al. disclose that a controller IC is generally configured to control current supplied to a transmitter (Figure 7 shows controller 68 coupled to current control 64, for example), but Chan et al. do not disclose specifically controlling alternating current supplied to the transmitter. However, King et al. teach that controller IC 50 (Figure 1) is configured to control AC modulation current supplied to a transmitter (column 7, lines 3-25).

Regarding claim 9 in particular, as well as the claim may be understood with respect to 35 U.S.C. 112 discussed above, King et al. further suggest providing the AC modulation current control signal to the laser via a digital to analog converter 24 (Figure 1).

Regarding claims 8 and 9, it would have been obvious to a person of ordinary skill in the art to specifically enable one of the controllers in the system described by Chan et al. in view of King et al. to control the modulation current supplied to the transmitter via a digital to analog converter, as taught by King et al., in order to provide specific control over the modulation current input to the laser.

Regarding claim 13, Chan et al. disclose that a controller IC is electrically coupled to a thermistor (i.e., a temperature sensor) disposed within the optoelectronic transceiver (column 7, lines 6-9).

Regarding claim 14, Chan et al. disclose a power source (such as power supply 8 shown in Figure 5). It would also be well understood in the art that the two controllers disclosed by Chan et al. inherently require connection to some source of power in order to function properly.

Regarding claims 15 and 17, Chan et al. in view of King et al. describe a system as discussed above with regard to claim 1. Chan et al. further disclose that a controller IC is generally configured to control current supplied to a transmitter (Figure 7 shows controller 68 coupled to current control 64, for example), but Chan et al. do not disclose specifically controlling direct current or alternating current supplied to the transmitter. However, King et al. teach that controller IC 50 (Figure 1) is configured to control DC bias current to a transmitter (column 6, lines 62-66; column 7, lines 26-31) and AC modulation current supplied to a transmitter (column 7, lines 3-25).

Regarding claims 15 and 17, it would have been obvious to a person of ordinary skill in the art to specifically enable one of the controllers in the system described by Chan et al. in view of King et al. to control the bias current or the modulation current supplied to the transmitter, as taught by King et al., in order to provide specific control over the two types of current input to the laser.

Examiner notes that although claims 15 and 17 recite “first controller IC” and “second controller IC” respectively, the claims each separately depend on claim 1, and not on each other. Therefore, the terms “first controller IC” and “second controller IC” in both claims 15 and 17 simply refer to “one of” the two controllers recited in claim 1.

Regarding claim 18, Chan et al. disclose one of the controller ICs is configured control a thermoelectric cooler in a transmitter optical subassembly (column 6, lines 63-66).

Regarding claim 19, Chan et al. in view of King et al. describe a system as discussed above with regard to claim 1 and Chan et al. further disclose that second controller comprises a microprocessor with logic that can execute stored programs. Although they do not specifically disclose first controller may include state machines, it is well understood in the art that the logic of a processor commonly includes state machines (i.e., some gates/logic for producing certain outputs when certain corresponding conditions are input). The claim does not recite further details regarding the state machines. It would have been obvious to a person of ordinary skill in the art to specifically include state machines in the first controller in the system described by Chan et al. in view of King et al. in order to allow the controller to process input signals and generate useful outputs based on the inputs.



Art Unit: 2633

8. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. in view of King et al. as applied to claims 1 and 2 above, and further in view of Jau et al. (US 6,205,505 B1).

Regarding claim 3, Chan et al. in view of King et al. describe a system as discussed above with regard to claims 1 and 2 including a serial interface, but they do not specifically disclose an I2C serial interface, a 2Wire serial interface, and an MDIO serial interface. However, different serial interfaces are well known in the art, as Jau et al. particularly suggest (column 3, lines 37-42), that are interchangeable with the RS232 serial interface already disclosed by Chan et al. It would have been obvious to a person of ordinary skill in the art to use a I2C serial interface, as suggested by Jau et al. for example, instead of the serial interface in the system described by Chan et al. in view of King et al. as an engineering design choice of a serial interface depending on the connected host and other equipment in the system. The claimed differences exist not as a result of an attempt by Applicants to solve an unknown problem but merely amount to the selection of expedients known as design choices to one of ordinary skill in the art.

9. Claims 7, 11, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. in view of King et al. as applied to claim 1 above, and further in view of Traa (US 6,222,660 B1).

Regarding claim 7, Chan et al. in view of King et al. describe a system as discussed above with regard to claim 1, but they do not specifically disclose that either controller IC is configured to control the power of the avalanche photodiode 112. However, Traa teaches a system related to the one disclosed by Chan et al. including an optoelectronic receiver (Figure 1).

Art Unit: 2633

Traa further teaches an avalanche photodiode (APD 10) coupled to an APD power supply (voltage supply 12) coupled to a controller IC 18 configured to supply an APD power supply control signal to the APD power supply causing the APD power supply to supply an APD voltage to the APD (column 2, lines 37-54). It would have been obvious to a person of ordinary skill in the art to include an avalanche photodiode power supply as taught by Traa in the system described by Chan et al. in view of King et al. in order to optimize the power of the optoelectronic receiver and thereby prevent excessive noise output (as Traa teaches; column 1, lines 5-39).

Further regarding claim 7, Chan et al. further disclose that a controller IC is generally configured to control current supplied to a transmitter (Figure 7 shows controller 68 coupled to current control 64, for example), but Chan et al. do not disclose specifically controlling direct current supplied to the transmitter. However, King et al. teach that controller IC 50 (Figure 1) is configured to control DC bias current to a transmitter (column 6, lines 62-66; column 7, lines 26-31).

Regarding claim 7, it would have been obvious to a person of ordinary skill in the art to specifically enable one of the controllers in the system described by Chan et al. in view of King et al. and Traa to control the bias current supplied to the transmitter, as taught by King et al., in order to provide specific control over the bias current input to the laser.

Regarding claim 11, Chan et al. in view of King et al. describe a system as discussed above with regard to claim 1. Chan et al. further disclose that a controller IC is coupled to a Thermoelectric Cooler (TEC) driver IC to receive a TEC temperature signal (column 6, lines 62-67; column 7, lines 1-10), but they do not specifically further disclose that either controller IC is

configured to control the power of the avalanche photodiode 112. However, Traa teaches a system related to the one disclosed by Chan et al. including an optoelectronic receiver (Figure 1). Traa further teaches an avalanche photodiode (APD 10) coupled to an APD power supply (voltage supply 12) coupled to a controller IC 18 configured to supply an APD power supply control signal to the APD power supply causing the APD power supply to supply an APD voltage to the APD (column 2, lines 37-54). It would have been obvious to a person of ordinary skill in the art to include an avalanche photodiode power supply as taught by Traa in the system described by Chan et al. in view of King et al. in order to optimize the power of the optoelectronic receiver and thereby prevent excessive noise output (as Traa teaches; column 1, lines 5-39).

Further regarding claim 11, Chan et al. in view of King et al. describe a system as discussed above with regard to claim 1 but Chan et al. do not specifically disclose that a controller IC is coupled to receive a direct current (DC) bias monitor signal and a laser diode monitor signal. However, King et al. further teach that a controller IC 50 (Figure 1) is coupled to a laser driver IC to receive a direct current (DC) bias monitor signal (from “average bias monitor” as shown in Figure 1; column 12, lines 33-37) and a laser diode monitor signal (from monitor photodiode 40; column 8, lines 10-24). It would have been obvious to a person of ordinary skill in the art to include a direct current bias monitor signal and a laser diode monitor signal as taught by King et al. in the system described by Chan et al. in view of King et al. in order to provide additional monitoring and feedback for optimizing the power output of the laser transmitter. Chan et al. already disclose that a controller IC (such as logic controller 28 in Figure 7) generally receives a laser monitor signal (from monitor photodiode 62).

Regarding claim 16, Chan et al. in view of King et al. describe a system as discussed above with regard to claim 1, but they do not specifically disclose that either controller IC is configured to control the power of the avalanche photodiode 112. However, Traa teaches a system related to the one disclosed by Chan et al. including an optoelectronic receiver (Figure 1). Traa further teaches an avalanche photodiode (APD 10) coupled to an APD power supply (voltage supply 12) coupled to a controller IC 18 configured to supply an APD power supply control signal to the APD power supply causing the APD power supply to supply an APD voltage to the APD (column 2, lines 37-54). It would have been obvious to a person of ordinary skill in the art to include an avalanche photodiode and APD power supply as taught by Traa in the system described by Chan et al. in view of King et al. in order to optimize the power of the optoelectronic receiver and thereby prevent excessive noise output (as Traa teaches; column 1, lines 5-39).

10. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. in view of King et al. as applied to claim 1 above, and further in view of Traa and Giebel et al. (US 5,926,303 A)

Regarding claim 10, Chan et al. in view of King et al. describe a system as discussed above with regard to claim 1, but they do not specifically disclose that either controller IC is configured to control the power of the avalanche photodiode 112. However, Traa teaches a system related to the one disclosed by Chan et al. including an optoelectronic receiver (Figure 1). Traa further teaches an avalanche photodiode (APD 10) coupled to an APD power supply (voltage supply 12) coupled to a controller IC 18 configured to supply an APD power supply control signal to the APD power supply causing the APD power supply to supply an APD

voltage to the APD (column 2, lines 37-54). It would have been obvious to a person of ordinary skill in the art to include an avalanche photodiode power supply as taught by Traa in the system described by Chan et al. in view of King et al. in order to optimize the power of the optoelectronic receiver and thereby prevent excessive noise output (as Traa teaches; column 1, lines 5-39).

Further regarding claim 10, Chan et al. in view of King et al. describe a system as discussed above with regard to claim 1 but Chan et al. do not specifically disclose that a controller IC is coupled to receive a direct current (DC) bias monitor signal and a laser diode monitor signal. However, King et al. further teach that a controller IC 50 (Figure 1) is coupled to a laser driver IC to receive a direct current (DC) bias monitor signal (from “average bias monitor” as shown in Figure 1; column 12, lines 33-37) and a laser diode monitor signal (from monitor photodiode 40; column 8, lines 10-24). It would have been obvious to a person of ordinary skill in the art to include a direct current bias monitor signal and a laser diode monitor signal as taught by King et al. in the system described by Chan et al. in view of King et al. in order to provide additional monitoring and feedback for optimizing the power output of the laser transmitter. Chan et al. already disclose that a controller IC (such as logic controller 28 in Figure 7) generally receives a laser monitor signal (from monitor photodiode 62).

Further regarding claim 10, Chan et al. in view of King et al. (and Traa) do not specifically suggest that the controller is connected to a post amplifier IC to receive a loss of received power signal.

However, Giebel et al. teach another optoelectronic transceiver related to the one already suggested by Chan et al. in view of King et al. and Traa, including an optical receiver (Figures 3

and 4). Giebel et al. further teach a receiving a loss of received power signal from a post amplifier IC (preamp 144 in Figure 4, which may be considered a “post amplifier” in the sense that is amplifies an electrical signal after opto-electrical conversion; column 10, lines 40-61). It would have been obvious to a person of ordinary skill in the art to include a post amplifier as taught by Giebel et al. the system described by Chan et al. in view of King et al. and Traa in order to detect when the received signal has been lost so that the system can respond to the potential fault.

11. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kollanyi et al. in view of Traa.

Regarding claim 21, Kollanyi et al. disclose a system as discussed above with regard to claim 20 and further disclose that that the optoelectronic receiver includes a photodetector 110, but they do not specifically disclose an avalanche photodiode coupled to a APD power supply. However, Traa teaches a system related to the one disclosed by Kollanyi et al. including an optoelectronic receiver (Figure 1). Traa further teaches an avalanche photodiode (APD 10) coupled to an APD power supply (voltage supply 12) coupled to a controller IC 18 configured to supply an APD power supply control signal to the APD power supply causing the APD power supply to supply an APD voltage to the APD (column 2, lines 37-54). It would have been obvious to a person of ordinary skill in the art to include an avalanche photodiode and APD power supply as taught by Traa in the system disclosed by Kollanyi et al. in order to optimize the power of the optoelectric receiver and thereby prevent excessive noise output (as Traa teaches; column 1, lines 5-39).

12. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kollanyi et al. in view of Thorton (US 2004/0202210 A1).

Regarding claim 22, Kollanyi et al. disclose a system as discussed above with regard to claim 20 and further disclose that the optoelectronic transmitter includes a temperature controller 140 (Figure 2), but they do not specifically disclose a thermoelectric cooler (TEC) and TEC driver. However, Thorton teaches a system related to the one disclosed by Kollanyi et al. including a transmitter controller (Figure 3). Thorton further teaches a thermoelectric cooler 326 (page 4, paragraph [0049]) coupled to a TEC driver (temperature control 342) coupled to a controller IC (i.e., "control unit" as shown in Figure 3) configured to supply a TEC control signal to the TEC driver causing the TEC driver to control the TEC. It would have been obvious to a person of ordinary skill in the art to include a temperature controller and driver as taught by Thorton in the system disclosed by Kollanyi et al. in order to stabilize the temperature of the laser and thereby stabilize the output of the transmitter.

***Allowable Subject Matter***

13. Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is a statement of reasons for the indication of allowable subject matter:

The prior art does not specifically disclose or fairly suggest a system including all the elements, steps, and limitations in the specific combination recited in claim 12 (and including claims 1 and 10 on which it depends), particularly wherein a first controller comprises at least one input port electrically coupled to an avalanche photodiode power supply to receive a

photodiode monitor signal; a post amplifier IC to receive a loss of received power signal; and a laser driver IC to receive a direct current (DC) bias monitor signal and a laser diode monitor signal; and a different, second controller receives the aforementioned photodiode monitor signal and the aforementioned DC bias monitor signal via an analog to digital converter.

*Conclusion*

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christina Y. Leung whose telephone number is 571-272-3023. The examiner can normally be reached on Monday to Friday, 6:30 to 3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on 571-272-3022. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christina Y Leung  
Christina Y Leung  
Patent Examiner  
Art Unit 2633